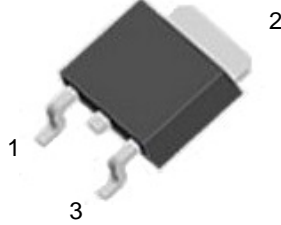
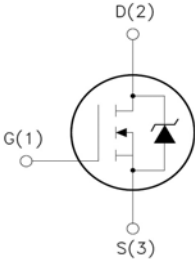


<p><b>CTKD60N04</b> 40V N-Channel MOSFET</p> <p><b>Features:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Low Intrinsic Capacitances.</li> <li><input type="checkbox"/> Excellent Switching Characteristics.</li> <li><input type="checkbox"/> Extended Safe Operating Area.</li> <li><input type="checkbox"/> Unrivalled Gate Charge :Qg= 29nC (Typ.).</li> <li><input type="checkbox"/> BVDSS=40V,I<sub>D</sub>=60A</li> <li><input type="checkbox"/> R<sub>DS(on)</sub> : 0.008Ω (Max) @V<sub>G</sub>=10V</li> <li><input type="checkbox"/> 100% Avalanche Tested</li> </ul>	<p>TO-252</p>   <p>1.Gate (G) 2.Drain (D) 3.Source (S)</p>
--	--

**Absolute Maximum Ratings** (Ta=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V <sub>DSS</sub>	Drain-Source Voltage	40	V
I <sub>D</sub>	Drain Current	T <sub>C</sub> =25°C	A
		T <sub>C</sub> =100°C	
V <sub>GS(TH)</sub>	Gate Threshold Voltage	±25	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (note5)	400	mJ
I <sub>AR</sub>	Avalanche Current (note2)	60	A
P <sub>D</sub>	Power Dissipation (Ta=25°C)	65	W
T <sub>j</sub>	Junction Temperature(Max)	175	°C
T <sub>stg</sub>	Storage Temperature	-55~+175	
TL	Maximum lead temperature for soldering purpose,1/8" from case for 5 seconds	300	

**Thermal Characteristics**

Symbol	Parameter	Typ.	Max.	Unit
R <sub>θJC</sub>	Thermal Resistance,Junction to Case	-	2.3	°C/W

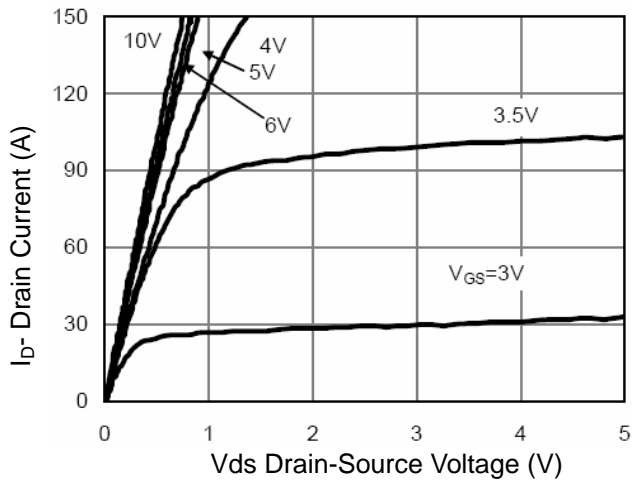
**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40	45	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	7.3	8	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=20A$	15	-	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	1800	-	PF
Output Capacitance	$C_{oss}$		-	280	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	190	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=2A, R_L=1\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	6.4	-	nS
Turn-on Rise Time	$t_r$		-	17.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29.6	-	nS
Turn-Off Fall Time	$t_f$		-	16.8	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=20V, I_D=20A,$ $V_{GS}=10V$	-	29	-	nC
Gate-Source Charge	$Q_{gs}$		-	4.5	-	nC
Gate-Drain Charge	$Q_{gd}$		-	6.4	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	60	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = 20A$ $di/dt = 100A/\mu s$ (Note3)	-	29	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	26	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

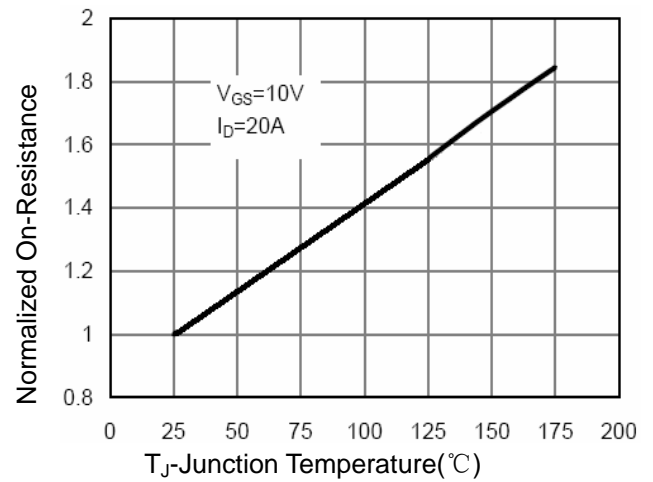
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition :  $T_J=25^\circ\text{C}, V_{DD}=20V, V_G=10V, L=1\text{mH}, R_G=25\Omega$ .

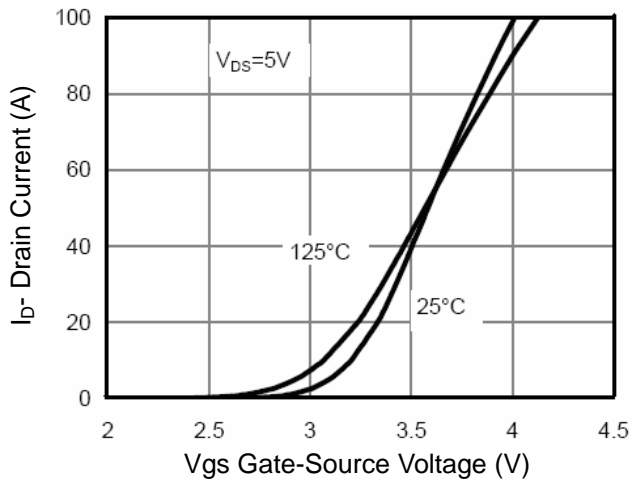
## Typical Characteristics



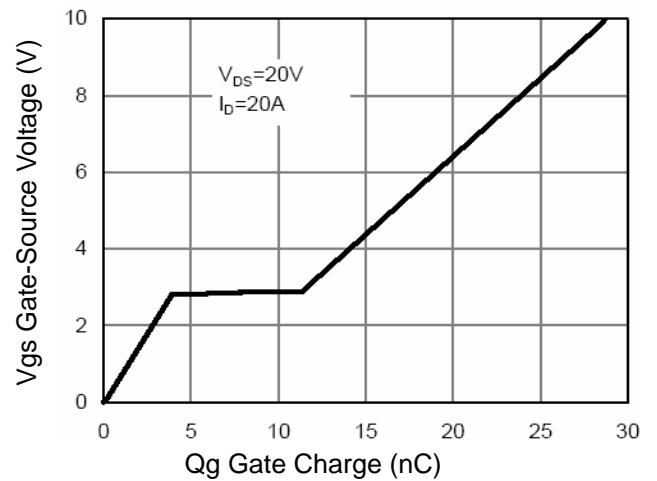
**Figure 1 Output Characteristics**



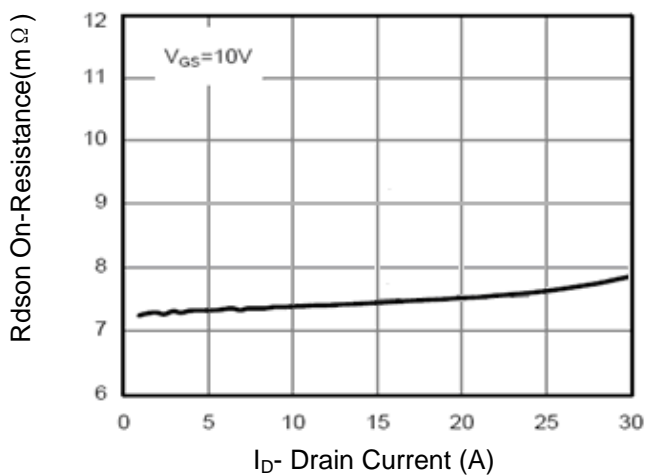
**Figure 4 Rdson-Junction Temperature**



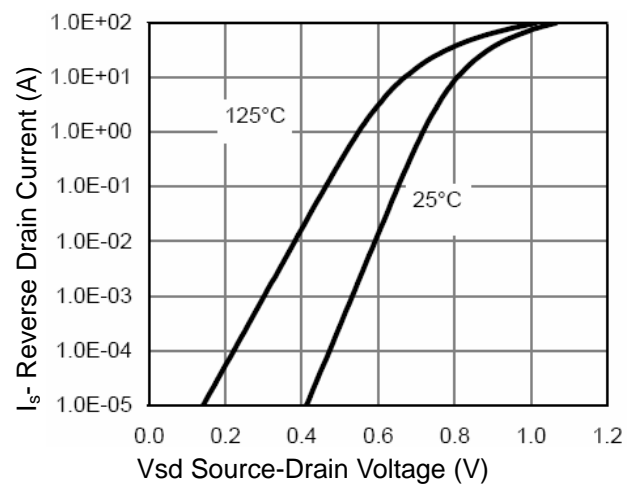
**Figure 2 Transfer Characteristics**



**Figure 5 Gate Charge**

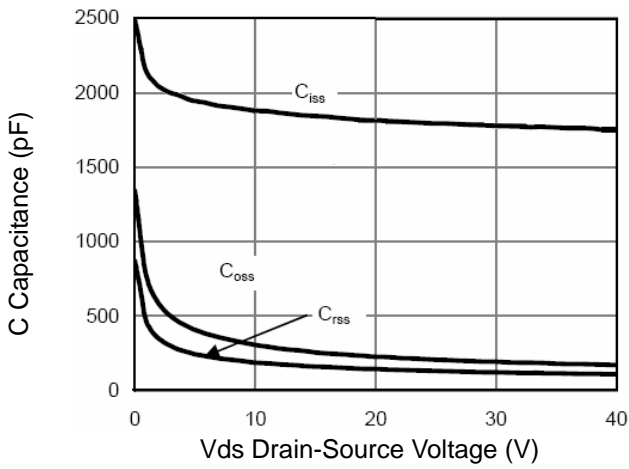


**Figure 3 Rdson- Drain Current**

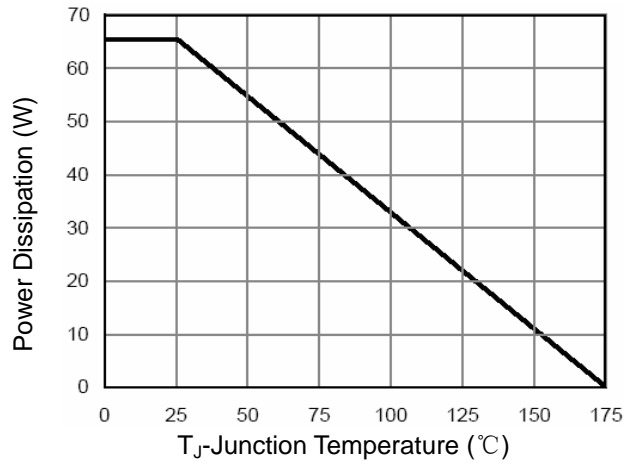


**Figure 6 Source- Drain Diode Forward**

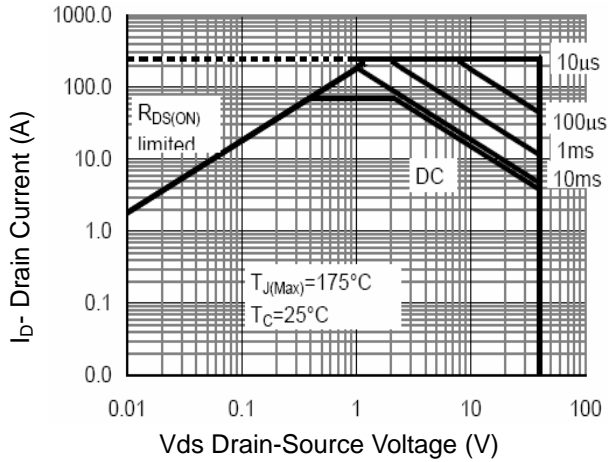
#### Typical Characteristics (Continued)



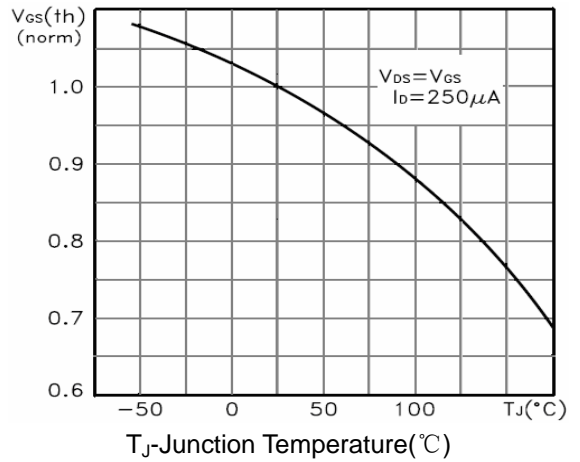
**Figure 7 Capacitance vs Vds**



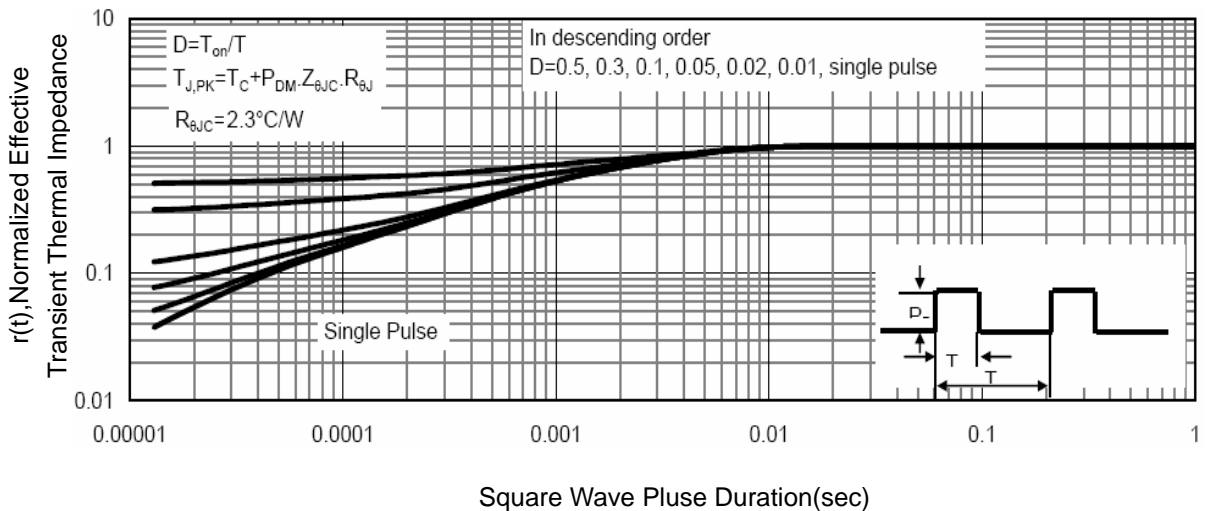
**Figure 9 Power De-rating**



**Figure 8 Safe Operation Area**

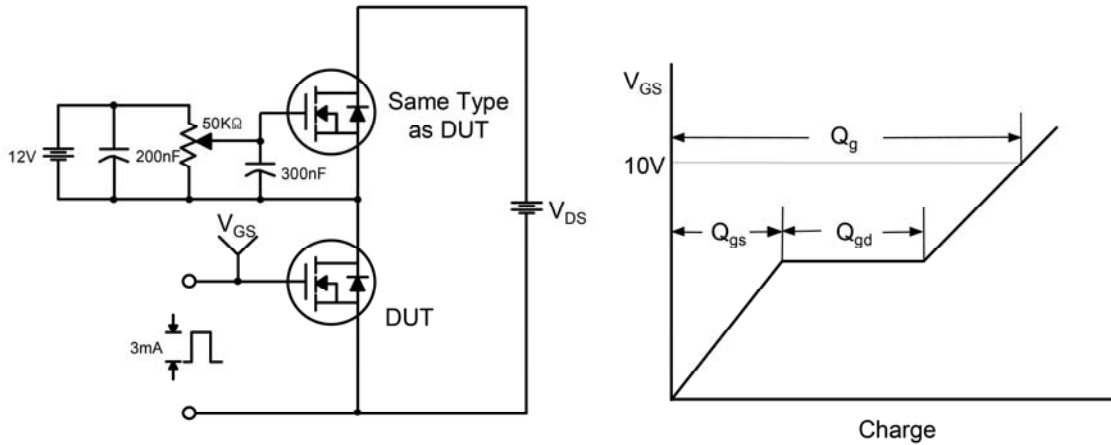


**Figure 10 V<sub>GS(th)</sub> vs Junction Temperature**

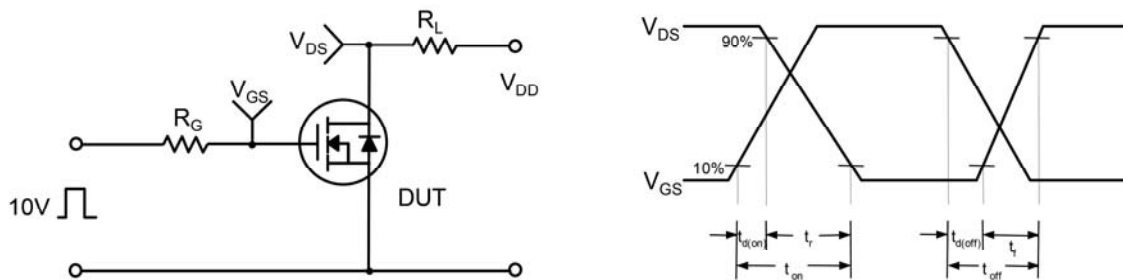


**Figure 11 Normalized Maximum Transient Thermal Impedance**

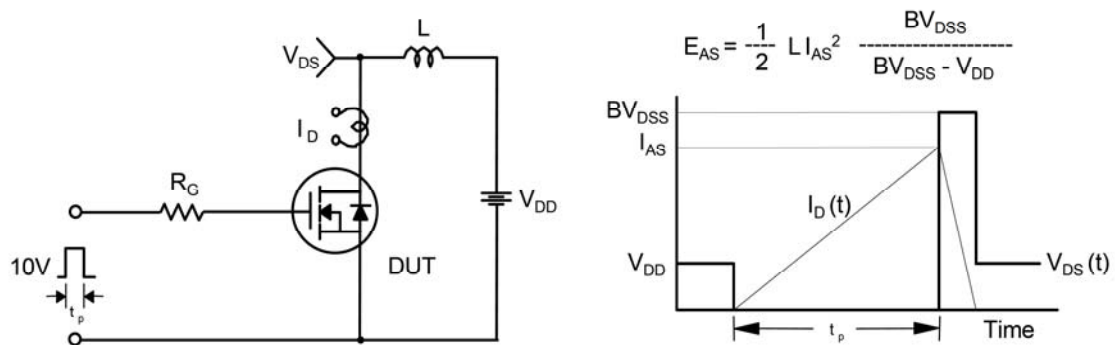
## Gate Charge Test Circuit & Waveform



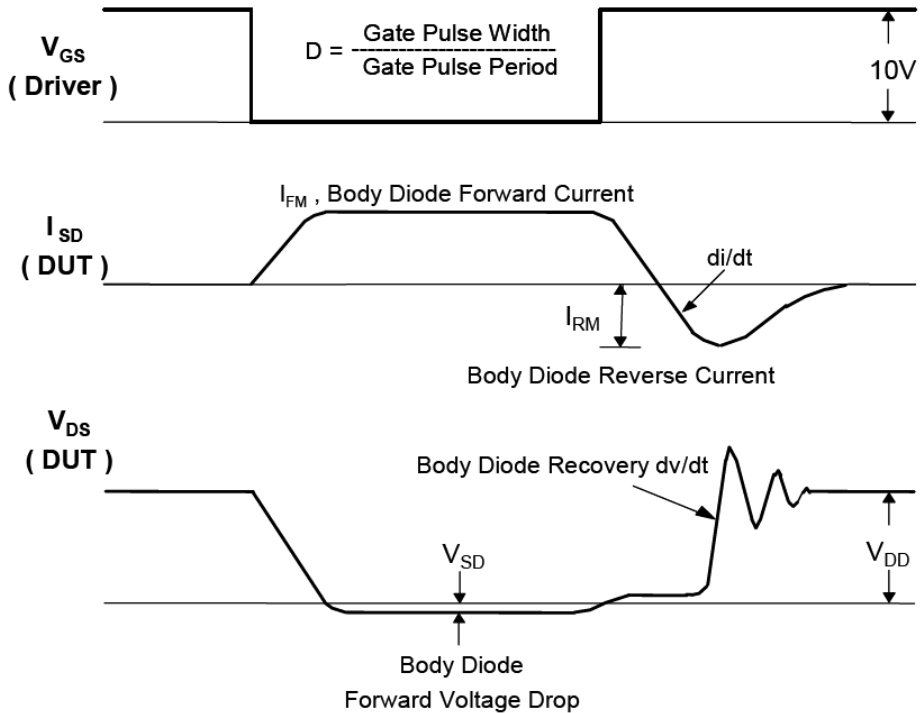
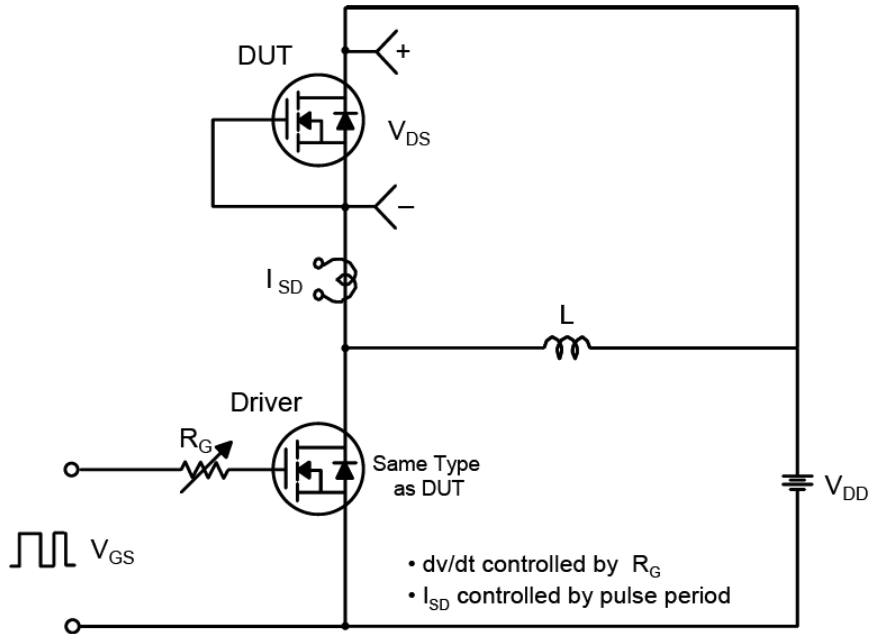
## Resistive Switching Test Circuit & Waveforms



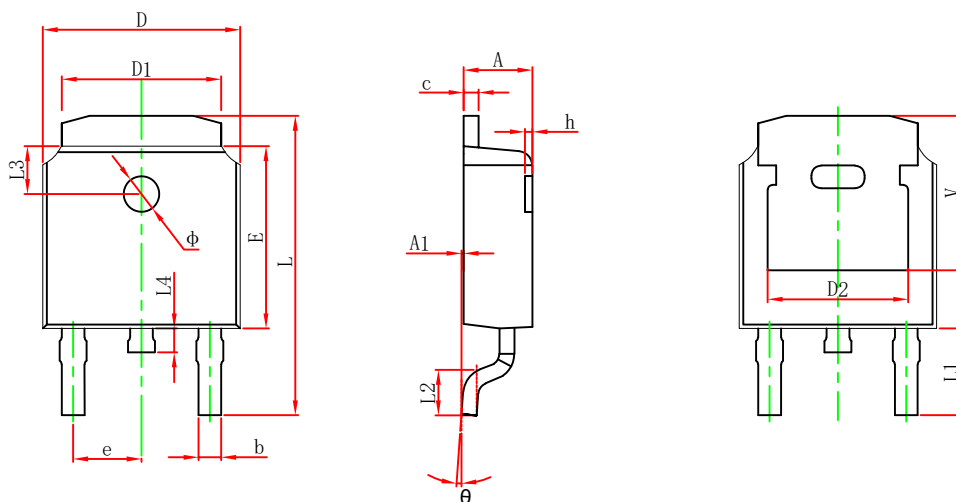
## Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveform

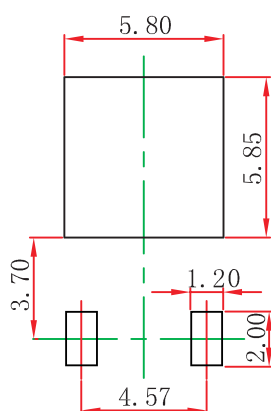


### Package Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.700	0.860	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.300	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
$\Phi$	1.100	1.300	0.043	0.051
$\theta$	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

### TO-252-2L Suggest Pad Layout



**NOTE:**

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.05\text{mm}$ .
3. The pad layout is for reference purposes only.