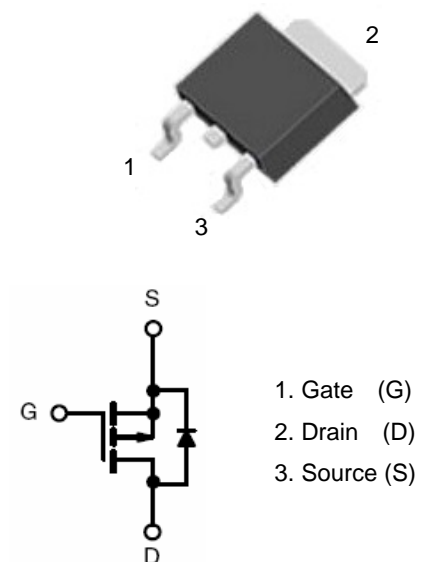


<p><b>CTKD30P06</b> 60V P-Channel MOSFET</p> <p><b>Features:</b></p> <ul style="list-style-type: none"> <li><input type="checkbox"/> Low Intrinsic Capacitances.</li> <li><input type="checkbox"/> Excellent Switching Characteristics.</li> <li><input type="checkbox"/> Extended Safe Operating Area.</li> <li><input type="checkbox"/> Unrivalled Gate Charge :Qg= 46nC (Typ.).</li> <li><input type="checkbox"/> BVDSS=-60V,I<sub>D</sub>= -30A</li> <li><input type="checkbox"/> R<sub>DS(on)</sub> : 0.045Ω (Max) @V<sub>G</sub>=-10V</li> <li><input type="checkbox"/> 100% Avalanche Tested</li> </ul>	<p>TO-252</p>  <p>1. Gate (G) 2. Drain (D) 3. Source (S)</p>
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**Absolute Maximum Ratings\*** (T<sub>C</sub>=25°C Unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	-60	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous	I <sub>D</sub>	-30	A
Drain Current-Continuous(T <sub>C</sub> =100°C)	I <sub>D</sub> (100°C)	-17.7	A
Pulsed Drain Current	I <sub>DM</sub>	-60	A
Maximum Power Dissipation	P <sub>D</sub>	80	W
Derating factor		0.72	W/°C
Single pulse avalanche energy (Note 5)	E <sub>AS</sub>	300	mJ
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 To 150	°C

**Thermal Characteristics**

Thermal Resistance,Junction-to-Case(Note 2)	R <sub>θJC</sub>	1.4	°C/W
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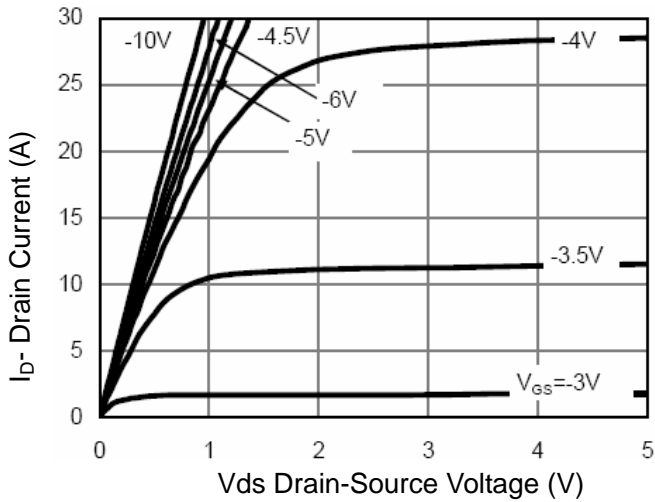
**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-	-2.	-3.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-20A$	-	39	45	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-10V, I_D=-10A$	-	25	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{ISS}$	$V_{DS}=-30V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	3430	-	PF
Output Capacitance	$C_{OSS}$		-	391	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	272	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=1.5\Omega,$ $V_{GS}=-10V, R_G=3\Omega$	-	12	-	nS
Turn-on Rise Time	$t_r$		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	38	-	nS
Turn-Off Fall Time	$t_f$		-	15	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-30V, I_D=-20A,$ $V_{GS}=-10V$	-	46	-	nC
Gate-Source Charge	$Q_{gs}$		-	9.5	-	nC
Gate-Drain Charge	$Q_{gd}$		-	10.5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=-10A$	-	-	-1.2	V
Diode Forward Current	$I_S$		-	-	-30	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = -10A$	-	47	-	nS
Reverse Recovery Charge	$Q_{rr}$	$di/dt = -100A/\mu s$ (Note3)	-	53	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

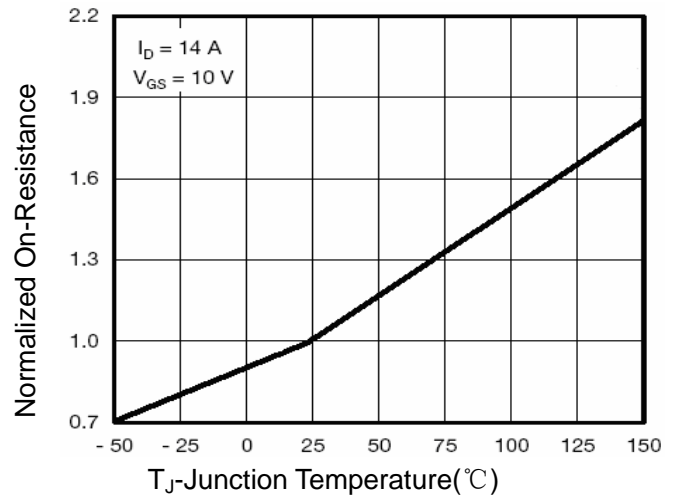
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^\circ\text{C}, V_{DD}=-20V, V_G=-10V, L=1\text{mH}, R_G=25\Omega, I_{AS}=33A$

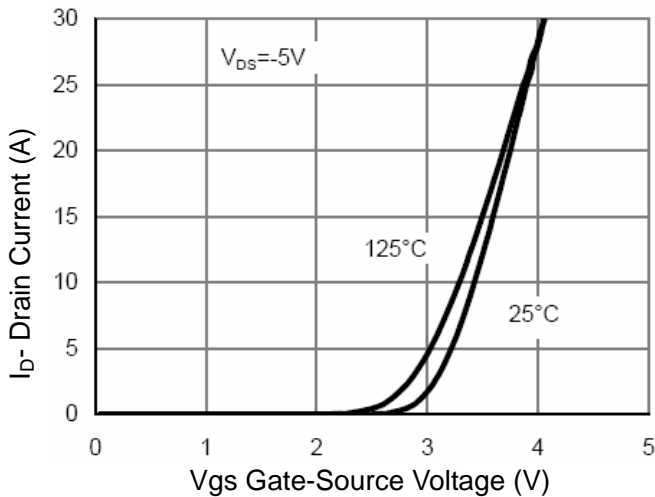
#### Typical Characteristics



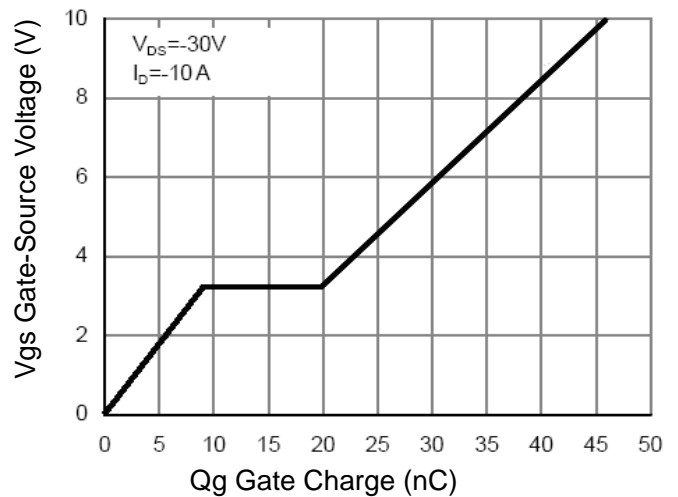
**Figure 1 Output Characteristics**



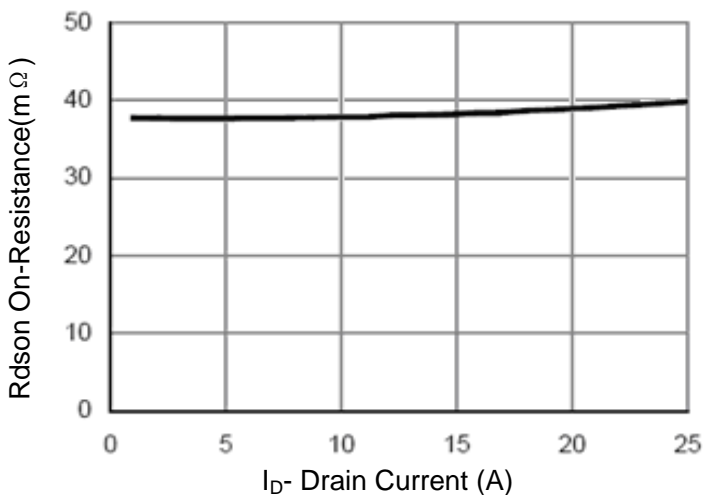
**Figure 4  $R_{dson}$ -Junction Temperature**



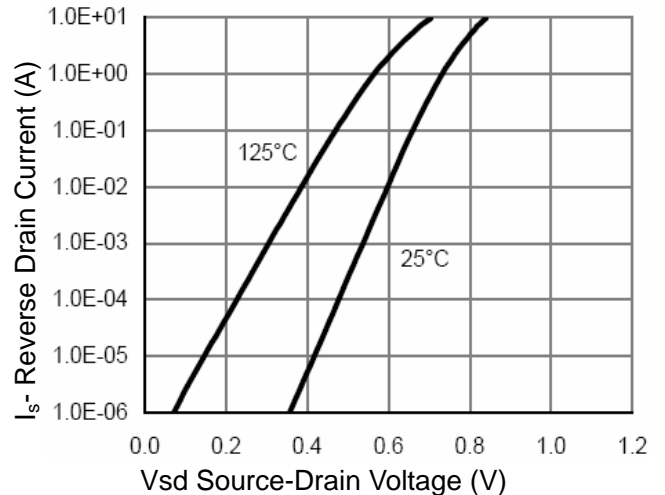
**Figure 2 Transfer Characteristics**



**Figure 5 Gate Charge**

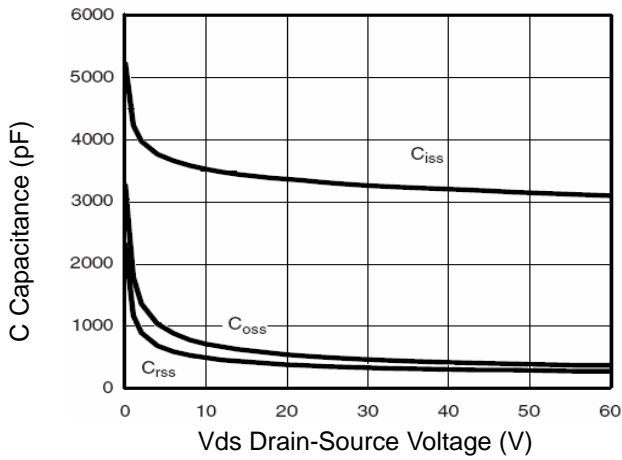


**Figure 3  $R_{dson}$ - Drain Current**

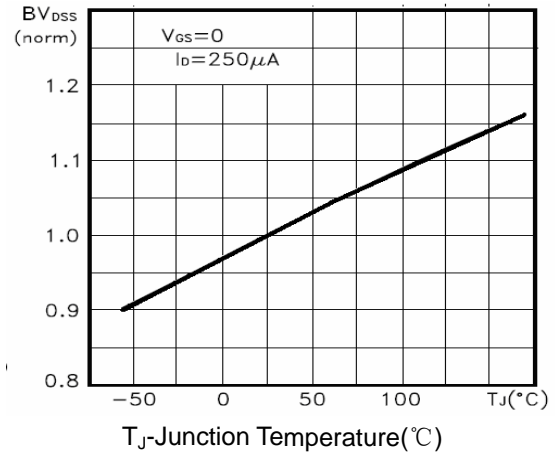


**Figure 6 Source- Drain Diode Forward**

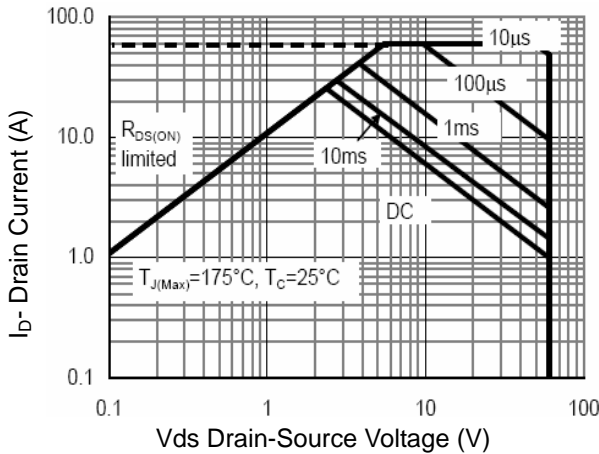
#### Typical Characteristics (Continued)



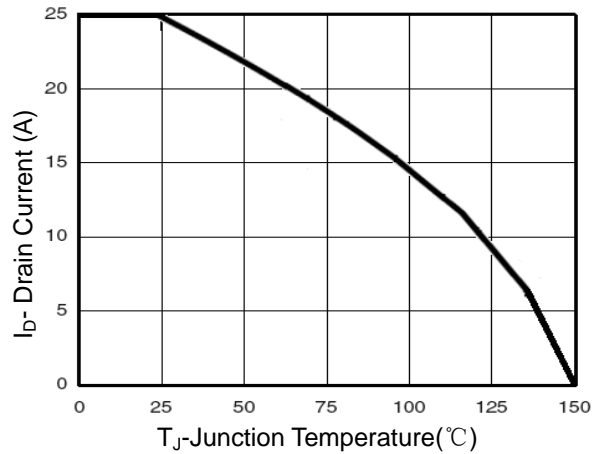
**Figure 7 Capacitance vs Vds**



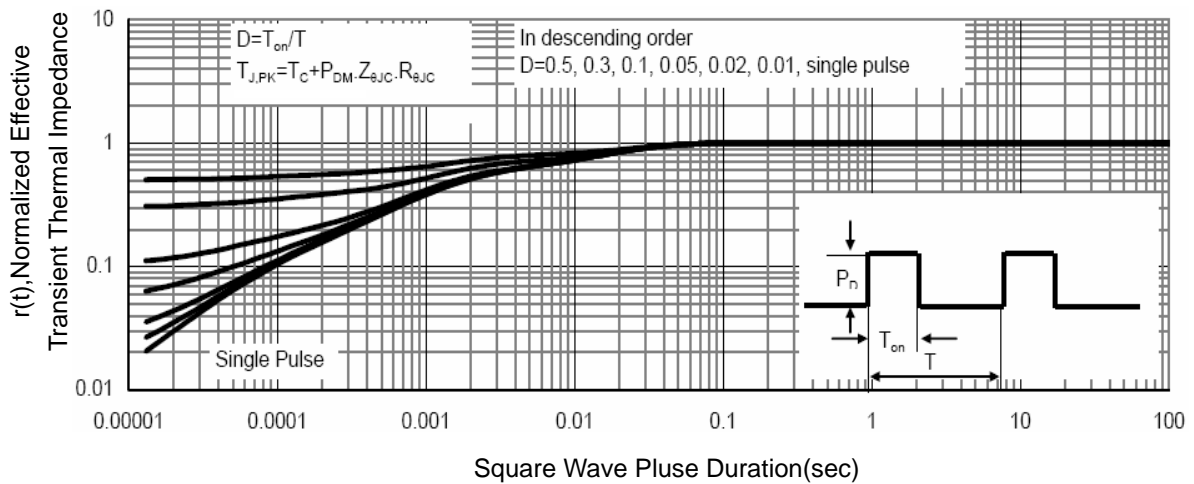
**Figure 9 BV<sub>DSS</sub> vs Junction Temperature**



**Figure 8 Safe Operation Area**



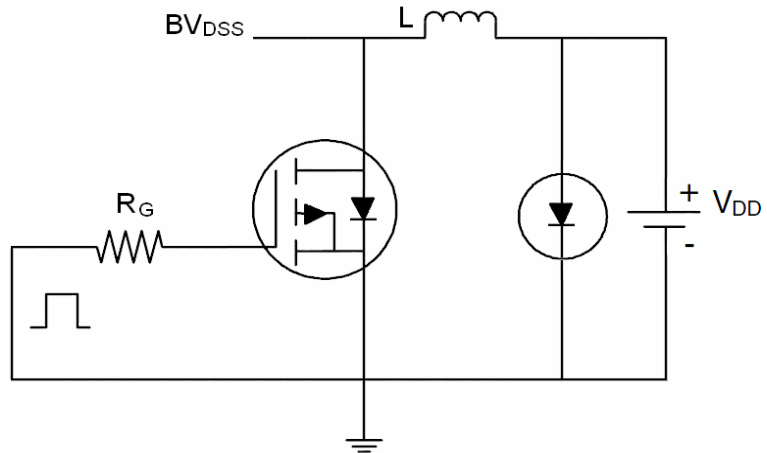
**Figure 10 ID Current De-rating**



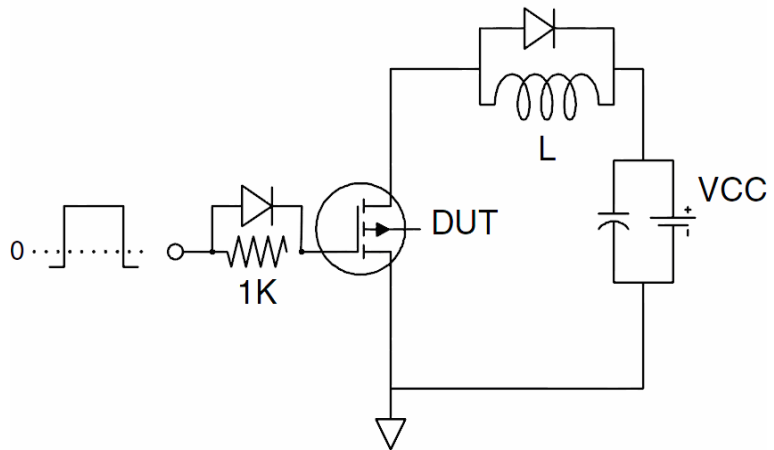
**Figure 11 Normalized Maximum Transient Thermal Impedance**

### Test Circuit

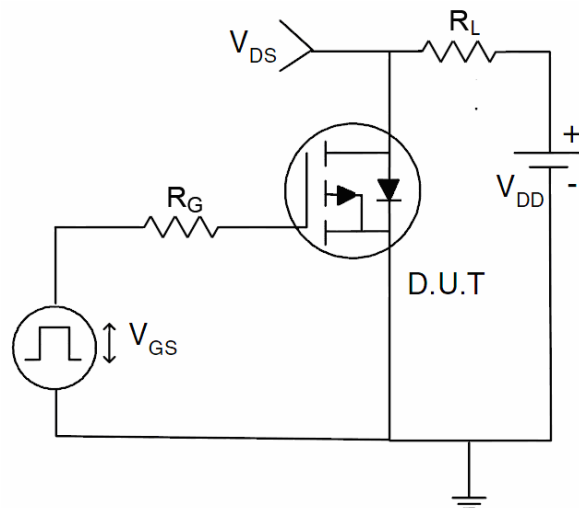
#### 1) $I_{AS}$ Test Circuit



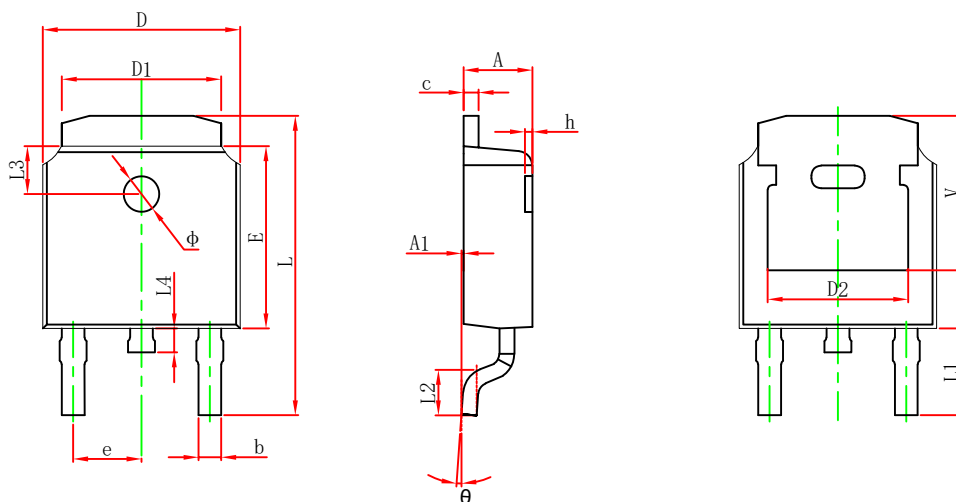
#### 2) Gate Charge Test Circuit



#### 3) Switch Time Test Circuit

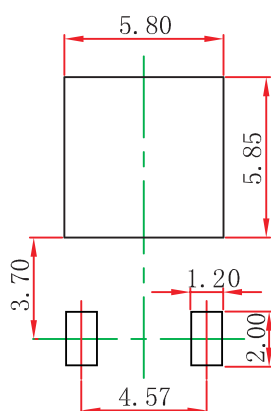


## Package Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.700	0.860	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.300	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

## TO-252-2L Suggest Pad Layout



### NOTE:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.05\text{mm}$ .
3. The pad layout is for reference purposes only.